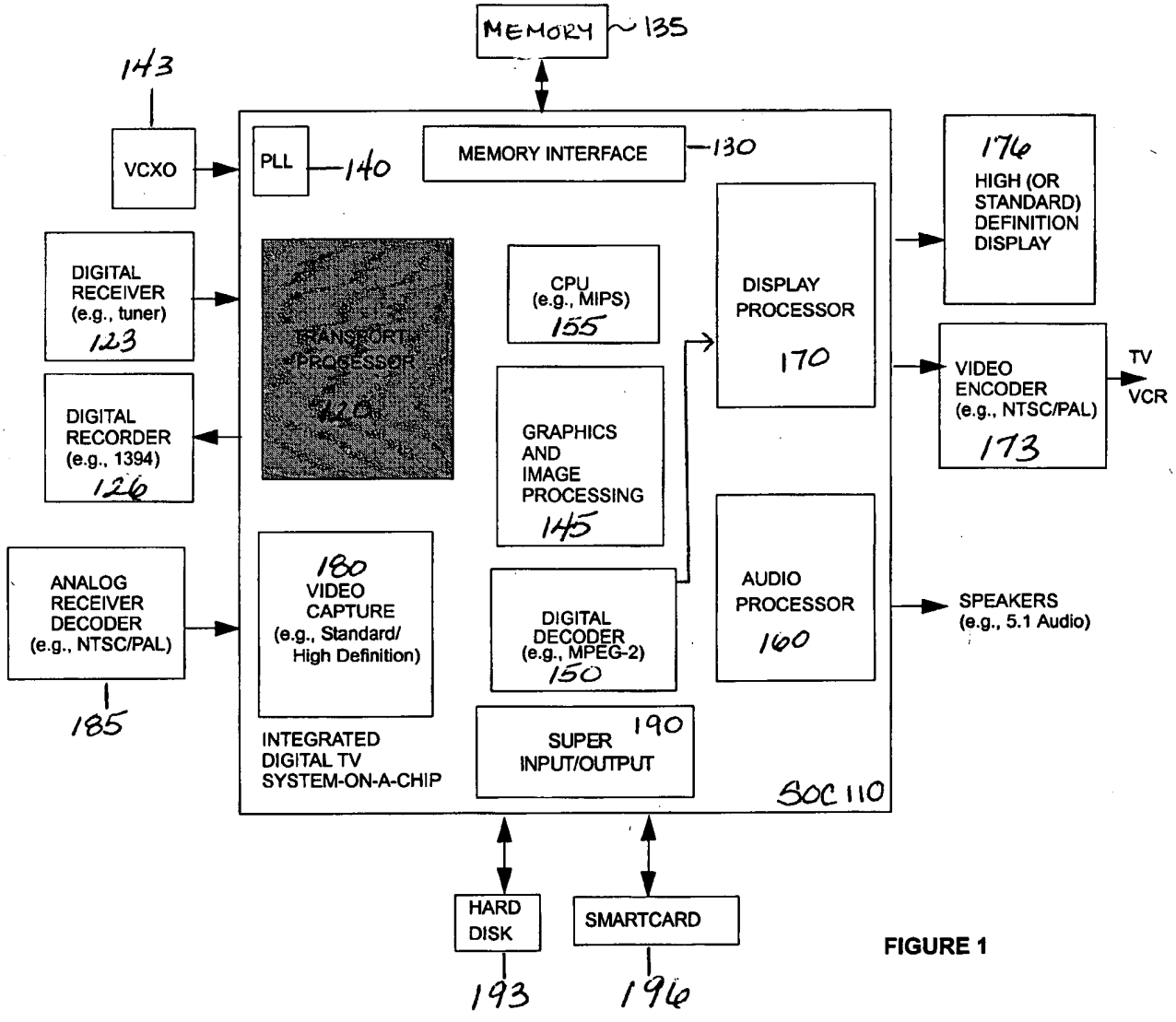

MEMORY
135
143
VCXO
PLL
140
MEMORY INTERFACE
130
176
HIGH (OR STANDARD) DEFINITION DISPLAY
DIGITAL RECEIVER (e.g., tuner)
123
TRANSPORT PROCESSOR
120
CPU (e.g., MIPS)
155
DISPLAY PROCESSOR
170
VIDEO ENCODER (e.g., NTSC/PAL)
173
TV
VCR
DIGITAL RECORDER (e.g., 1394)
126
GRAPHICS AND IMAGE PROCESSING
145
ANALOG RECEIVER DECODER (e.g., NTSC/PAL)
185
180
VIDEO CAPTURE (e.g., Standard/ High Definition)
DIGITAL DECODER (e.g., MPEG-2)
150
AUDIO PROCESSOR
160
SPEAKERS (e.g., 5.1 Audio)
INTEGRATED DIGITAL TV SYSTEM-ON-A-CHIP
190
SUPER INPUT/OUTPUT
SOC 110
HARD DISK
193
SMARTCARD
196

FIGURE 1

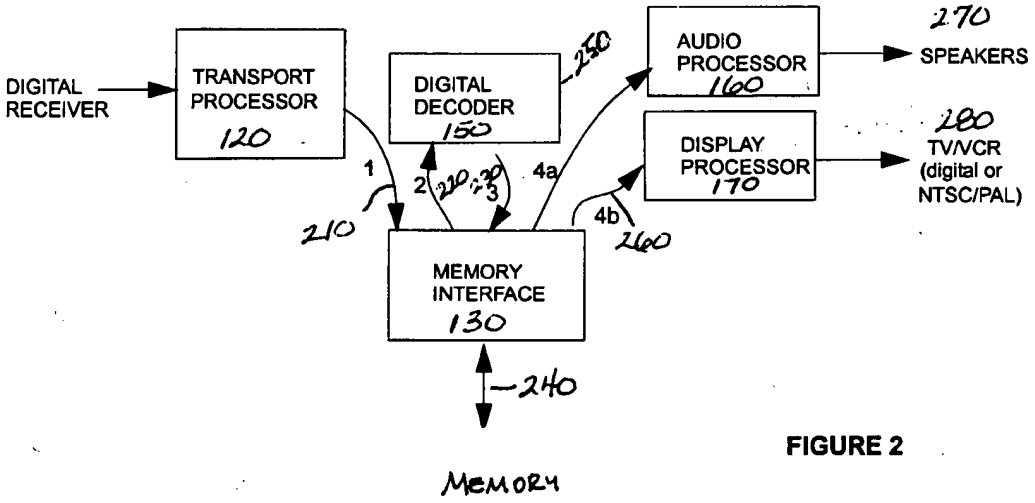


FIGURE 2

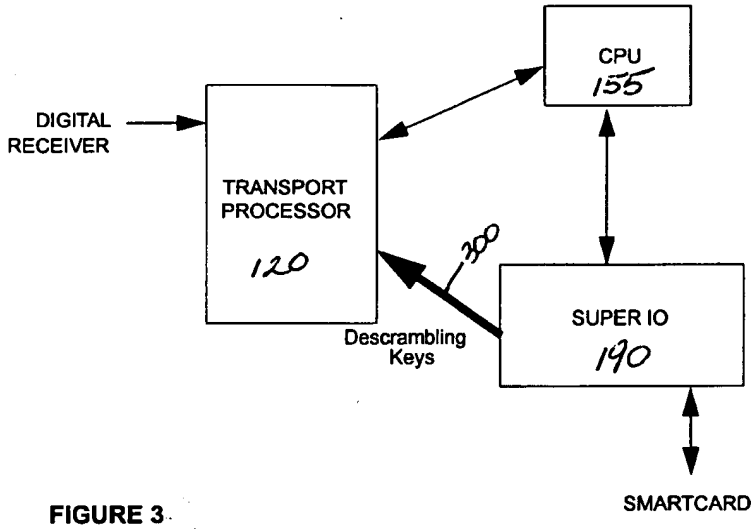


FIGURE 3

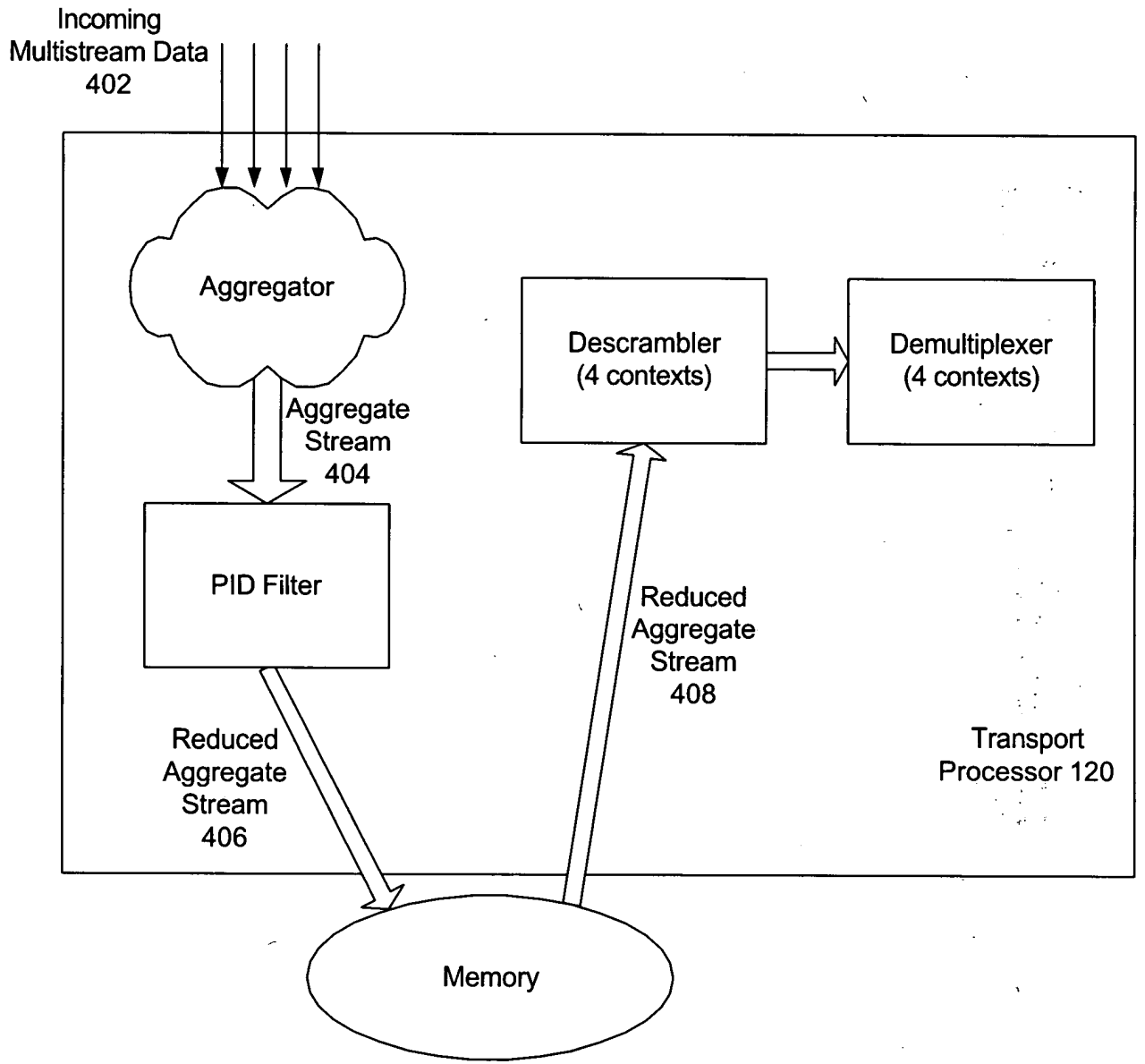

Incoming
Multistream Data
402
Aggregator
Aggregate
Stream
404
PID Filter
Reduced
Aggregate
Stream
406
Descrambler
(4 contexts)
Demultiplexer
(4 contexts)
Reduced
Aggregate
Stream
408
Transport
Processor 120
Memory

Fig. 4A

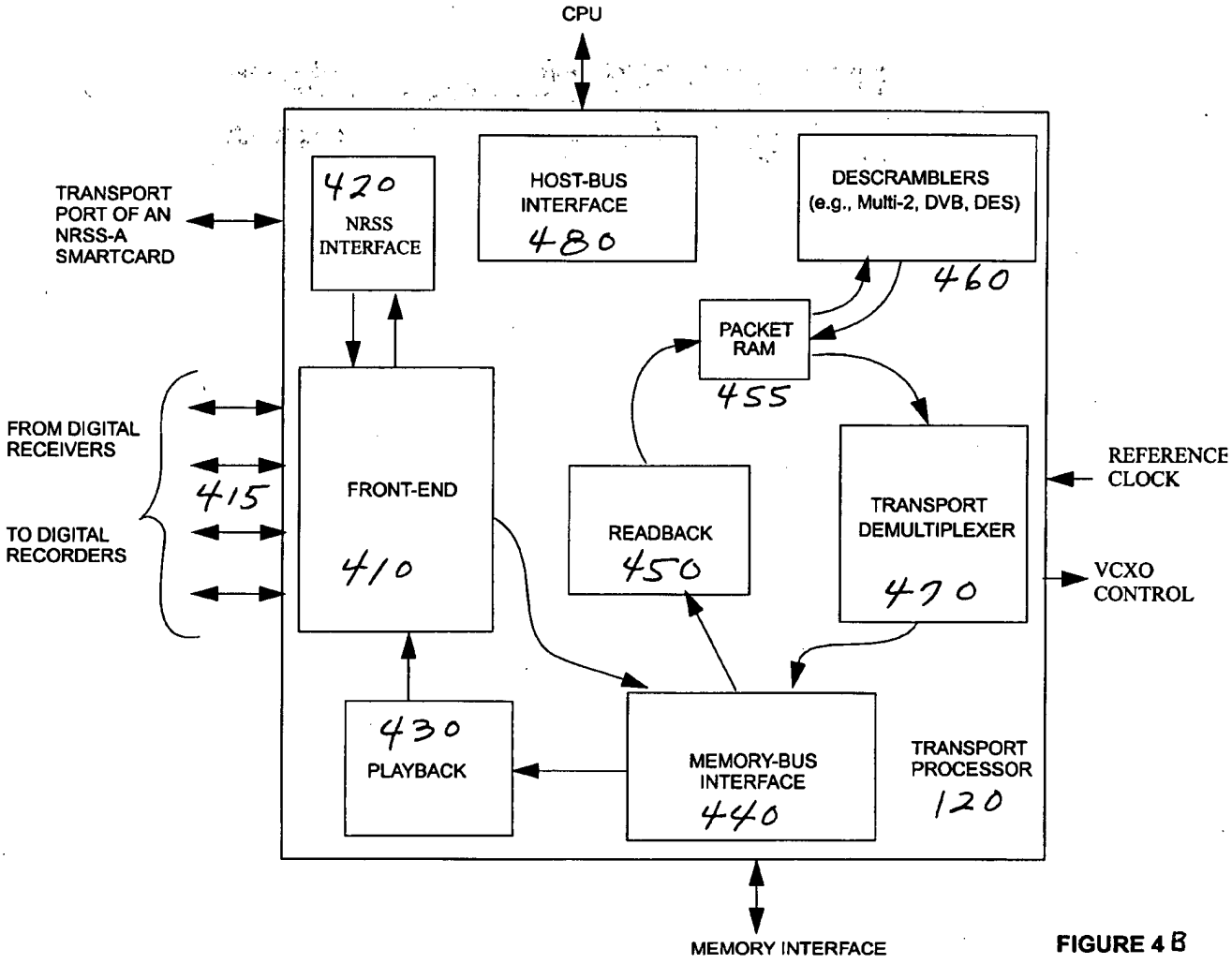

CPU
TRANSPORT PORT OF AN NRSS-A SMARTCARD
420
NRSS INTERFACE
HOST-BUS INTERFACE
480
DESCRAMBLERS (e.g., Multi-2, DVB, DES)
460
PACKET RAM
455
FROM DIGITAL RECEIVERS
TO DIGITAL RECORDERS
415
FRONT-END
410
READBACK
450
TRANSPORT DEMULTIPLEXER
470
REFERENCE CLOCK
VCXO CONTROL
430
PLAYBACK
MEMORY-BUS INTERFACE
440
TRANSPORT PROCESSOR
120
MEMORY INTERFACE

FIGURE 4 B

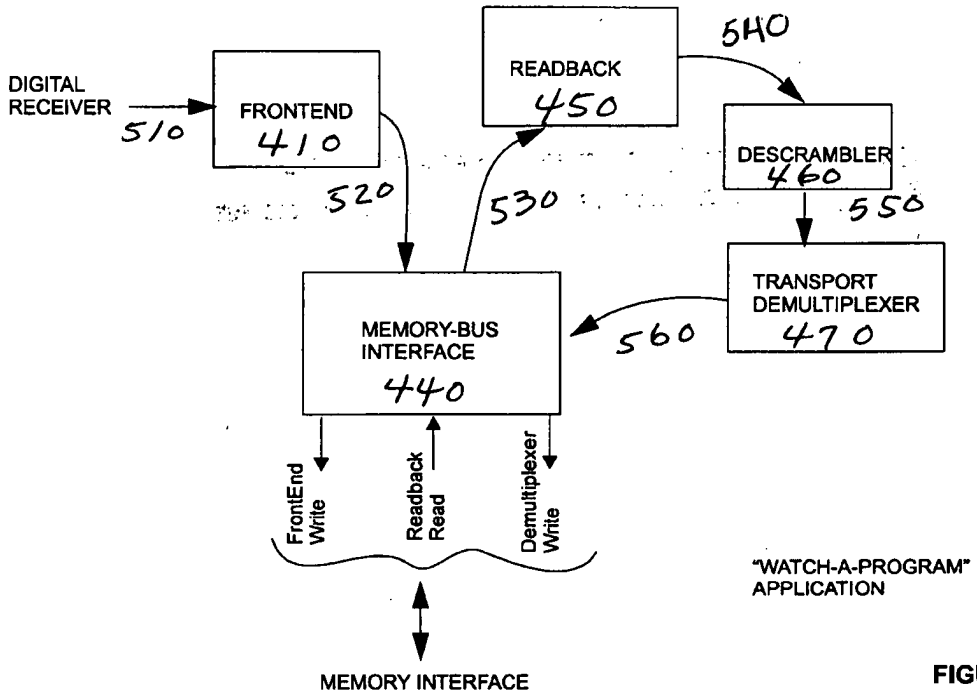

DIGITAL RECEIVER
510
FRONTEND
410
READBACK
450
540
DESCRAMBLER
460
520
530
550
TRANSPORT DEMULTIPLEXER
470
MEMORY-BUS INTERFACE
440
560
FrontEnd Write
Readback Read
Demultiplexer Write
"WATCH-A-PROGRAM" APPLICATION
MEMORY INTERFACE

FIGURE 5

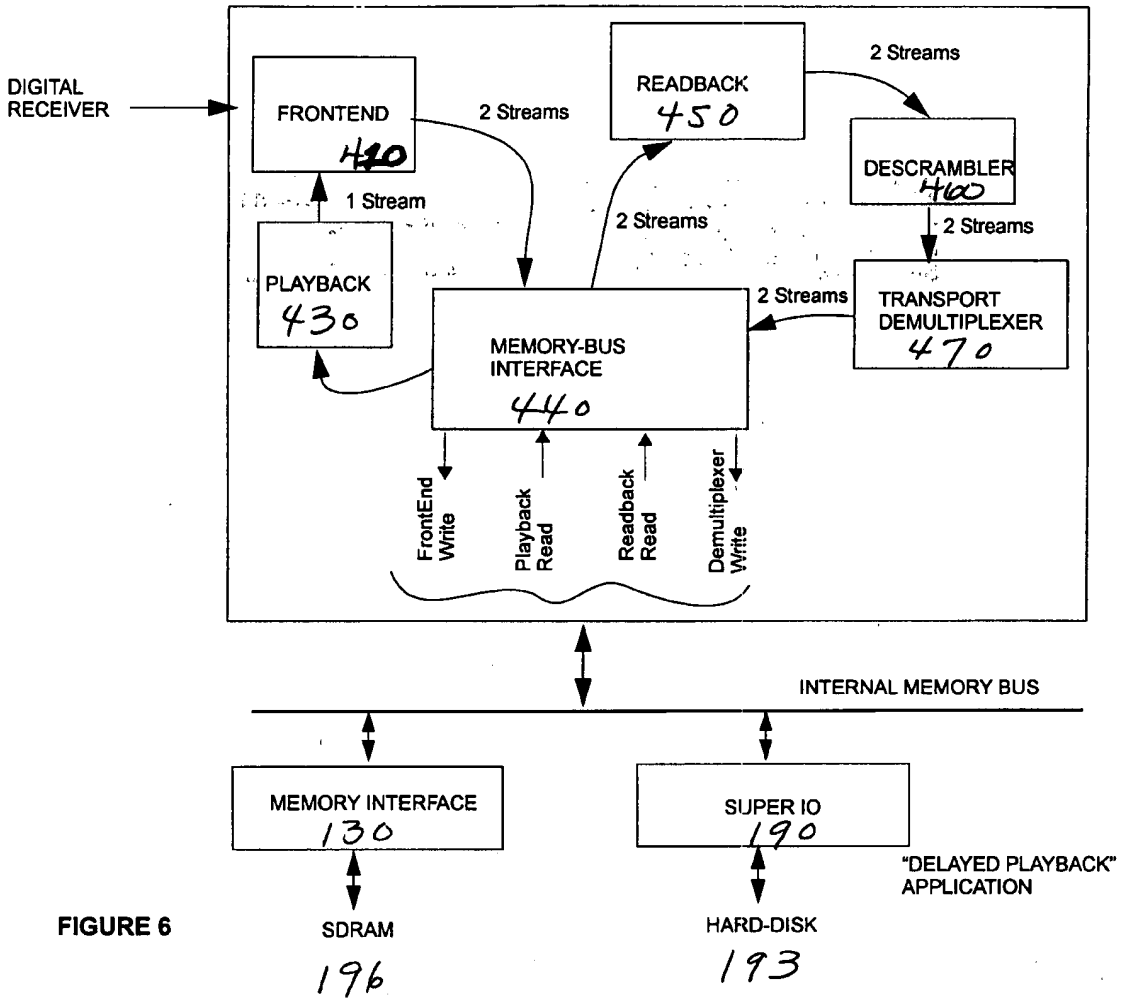

DIGITAL RECEIVER
FRONTEND
420
2 Streams
READBACK
450
2 Streams
DESCRAMBLER
460
2 Streams
1 Stream
PLAYBACK
430
2 Streams
MEMORY-BUS INTERFACE
440
2 Streams
TRANSPORT DEMULTIPLEXER
470
FrontEnd Write
Playback Read
Readback Read
Demultiplexer Write
INTERNAL MEMORY BUS
MEMORY INTERFACE
130
SUPER IO
190
"DELAYED PLAYBACK" APPLICATION
SDRAM
196
HARD-DISK
193

FIGURE 6

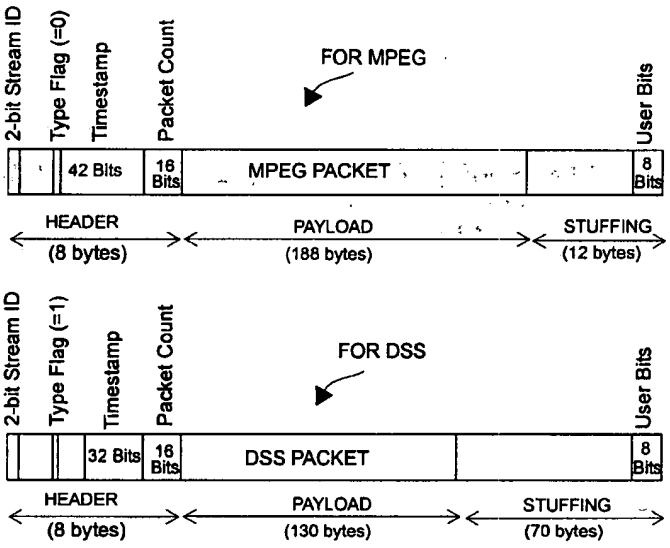


FIGURE 7

PROPRIETARY 208-BYTE PACKET FORMAT

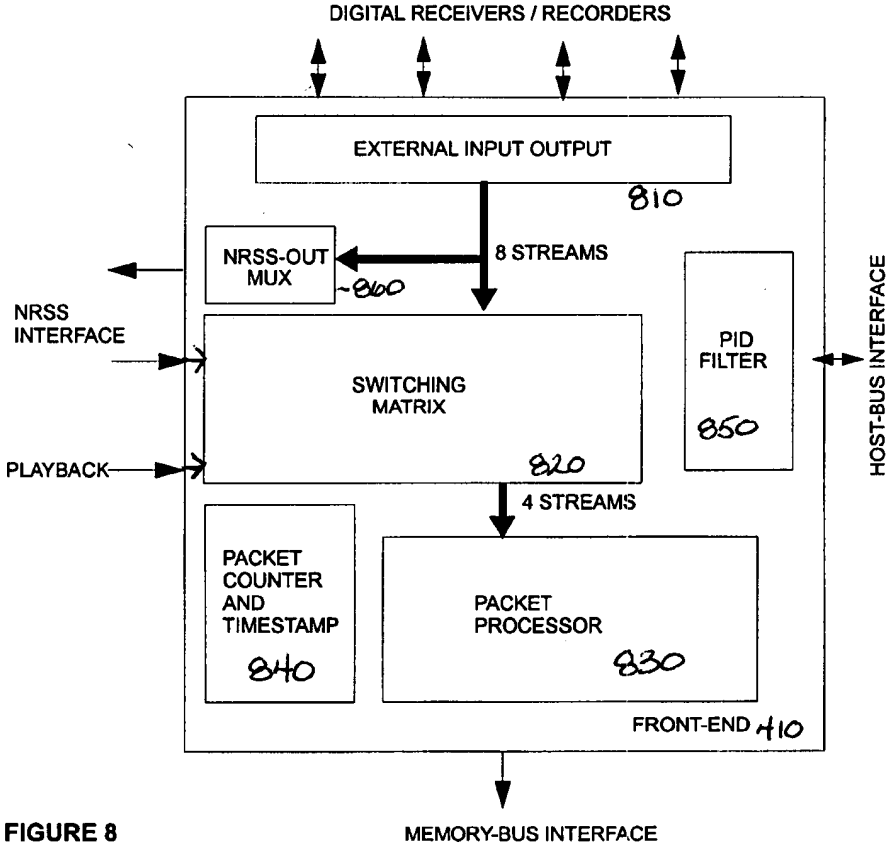


FIGURE 8

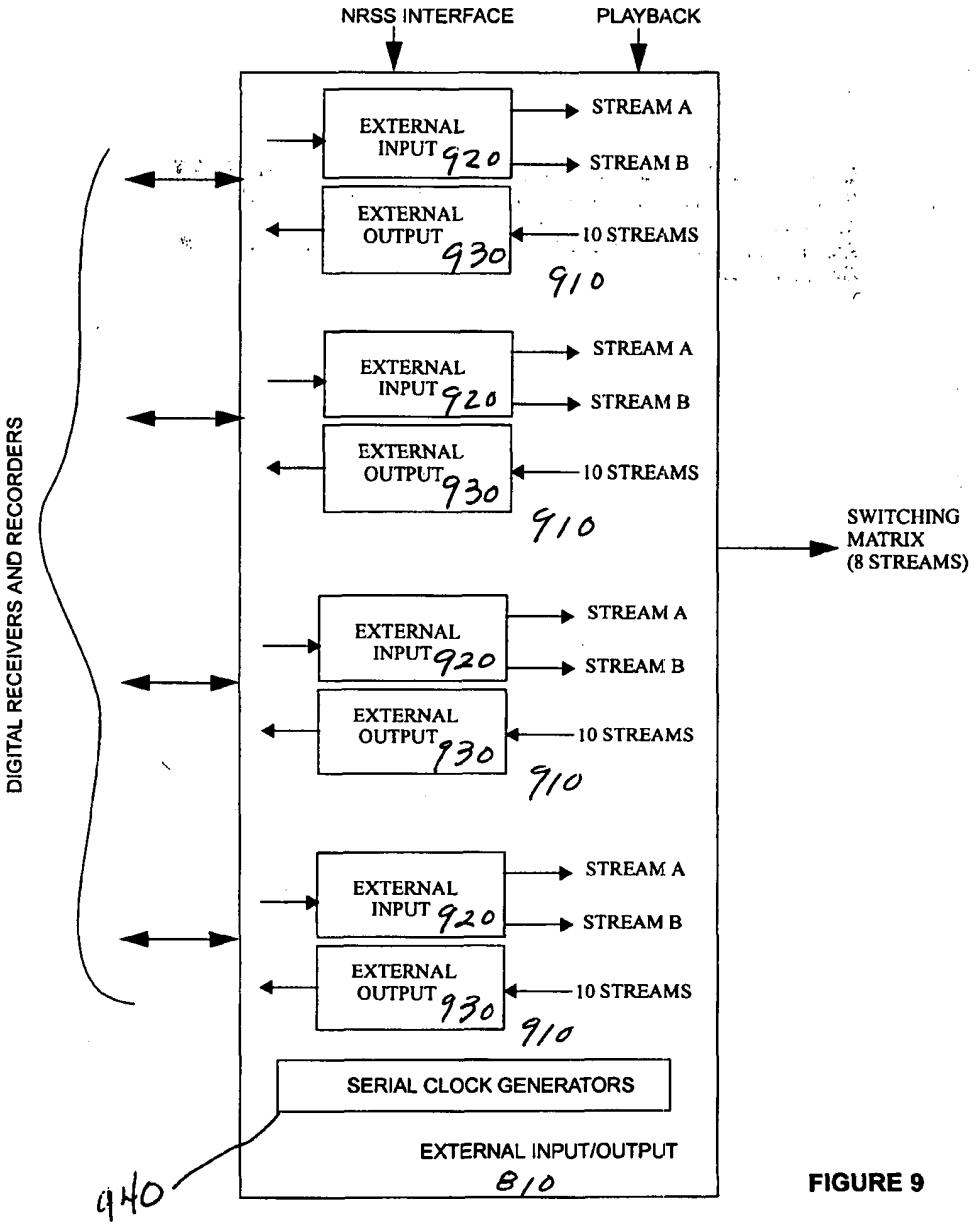

NRSS INTERFACE
PLAYBACK
EXTERNAL INPUT 920
STREAM A
STREAM B
EXTERNAL OUTPUT 930
10 STREAMS
910
EXTERNAL INPUT 920
STREAM A
STREAM B
EXTERNAL OUTPUT 930
10 STREAMS
910
EXTERNAL INPUT 920
STREAM A
STREAM B
EXTERNAL OUTPUT 930
10 STREAMS
910
EXTERNAL INPUT 920
STREAM A
STREAM B
EXTERNAL OUTPUT 930
10 STREAMS
910
SERIAL CLOCK GENERATORS
940
EXTERNAL INPUT/OUTPUT
810
DIGITAL RECEIVERS AND RECORDERS
SWITCHING MATRIX (8 STREAMS)

FIGURE 9

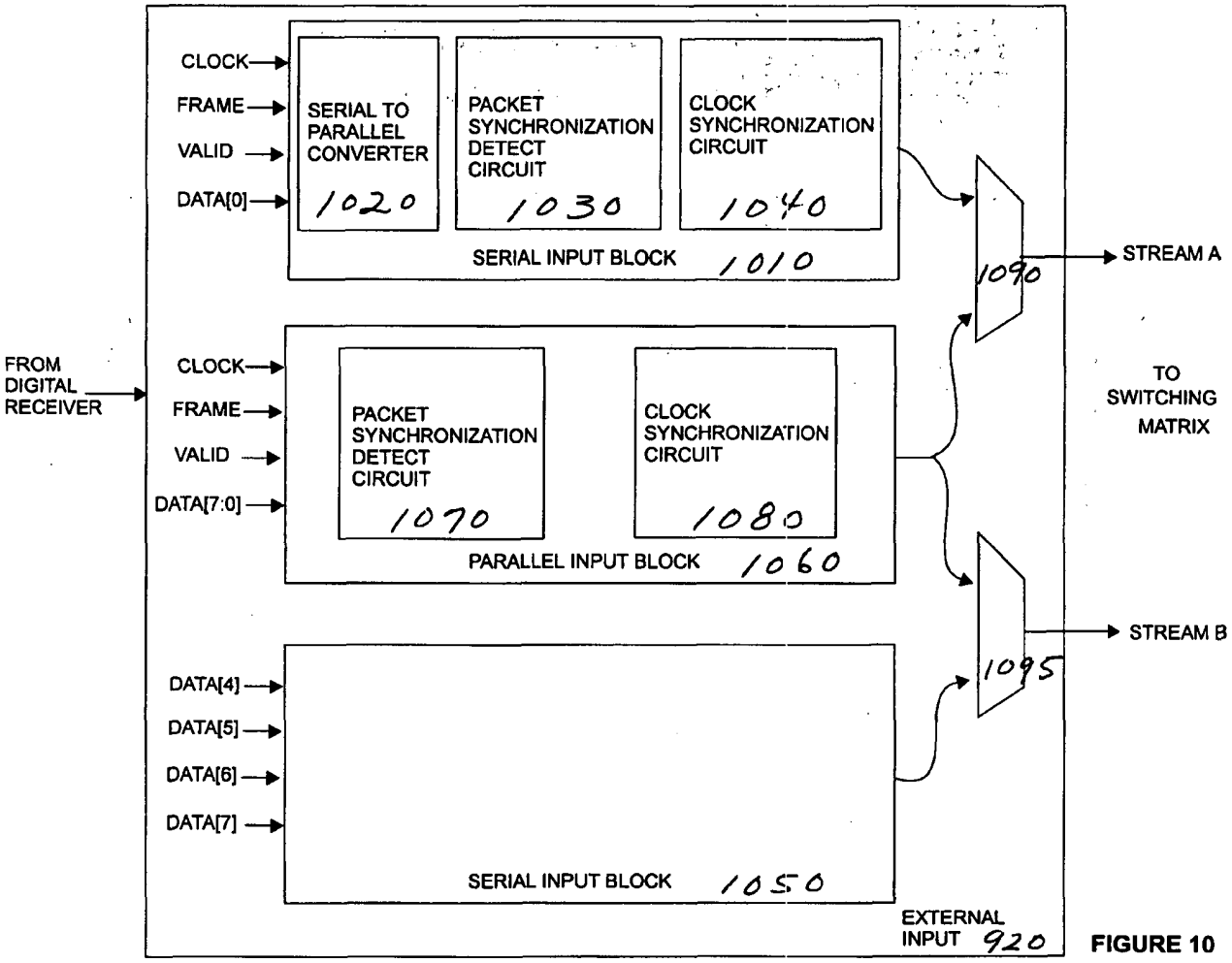

CLOCK
FRAME
VALID
DATA[0]
SERIAL TO PARALLEL CONVERTER
1020
PACKET SYNCHRONIZATION DETECT CIRCUIT
1030
CLOCK SYNCHRONIZATION CIRCUIT
1040
SERIAL INPUT BLOCK
1010
1090
STREAM A
FROM DIGITAL RECEIVER
CLOCK
FRAME
VALID
DATA[7:0]
PACKET SYNCHRONIZATION DETECT CIRCUIT
1070
CLOCK SYNCHRONIZATION CIRCUIT
1080
PARALLEL INPUT BLOCK
1060
TO SWITCHING MATRIX
DATA[4]
DATA[5]
DATA[6]
DATA[7]
SERIAL INPUT BLOCK
1050
1095
STREAM B
EXTERNAL INPUT
920

FIGURE 10

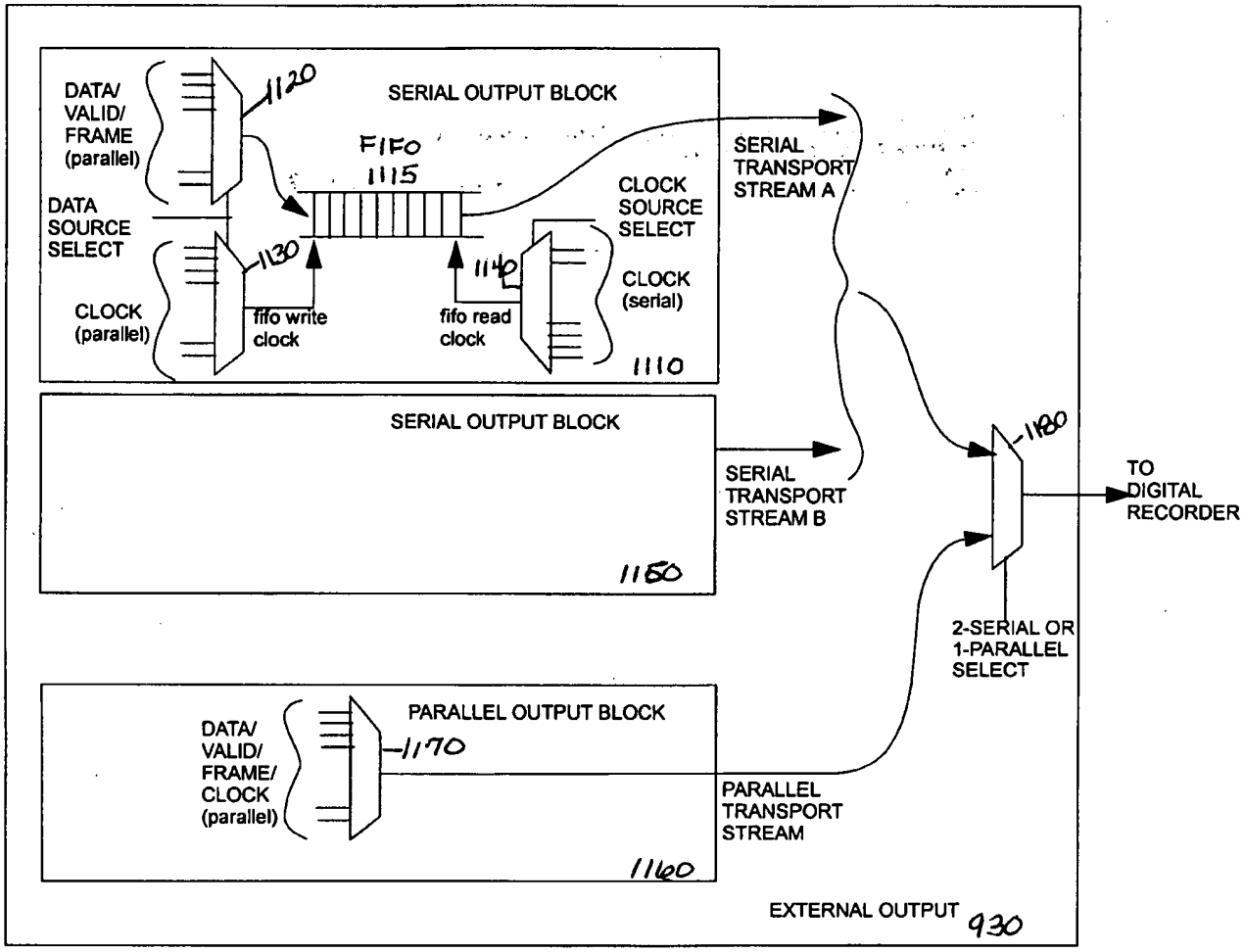

DATA/
VALID/
FRAME
(parallel)
1120
SERIAL OUTPUT BLOCK
FIFO
1115
DATA
SOURCE
SELECT
CLOCK
SOURCE
SELECT
1130
1140
CLOCK
(parallel)
fifo write
clock
fifo read
clock
CLOCK
(serial)
1110
SERIAL
TRANSPORT
STREAM A
SERIAL OUTPUT BLOCK
1150
SERIAL
TRANSPORT
STREAM B
1180
TO
DIGITAL
RECORDER
2-SERIAL OR
1-PARALLEL
SELECT
PARALLEL OUTPUT BLOCK
DATA/
VALID/
FRAME/
CLOCK
(parallel)
1170
1160
PARALLEL
TRANSPORT
STREAM
EXTERNAL OUTPUT
930

FIGURE 11

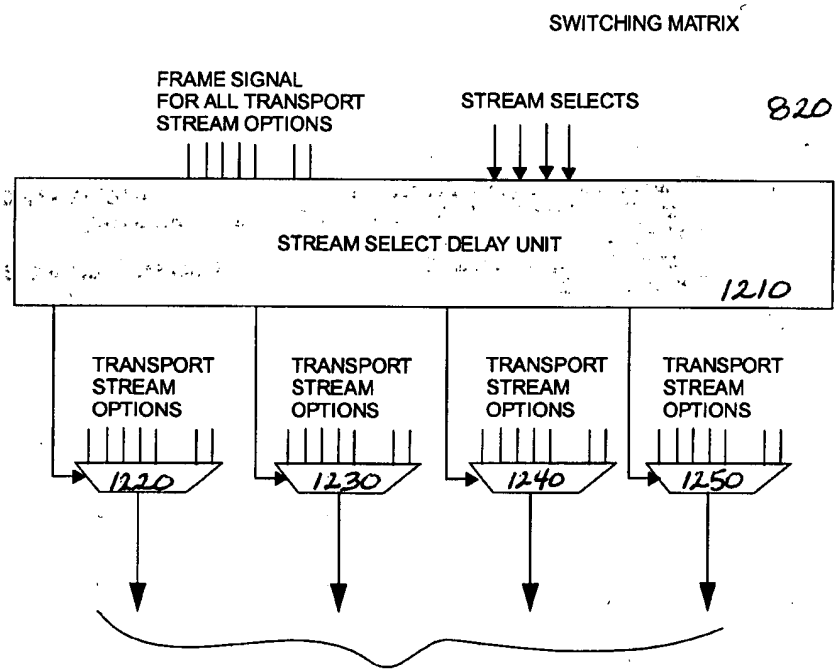

SWITCHING MATRIX
FRAME SIGNAL
FOR ALL TRANSPORT
STREAM OPTIONS
STREAM SELECTS
820
STREAM SELECT DELAY UNIT
1210
TRANSPORT
STREAM
OPTIONS
TRANSPORT
STREAM
OPTIONS
TRANSPORT
STREAM
OPTIONS
TRANSPORT
STREAM
OPTIONS
1220
1230
1240
1250
FOUR SELECTED STREAMS TO PACKET PROCESSOR

FIGURE 12A

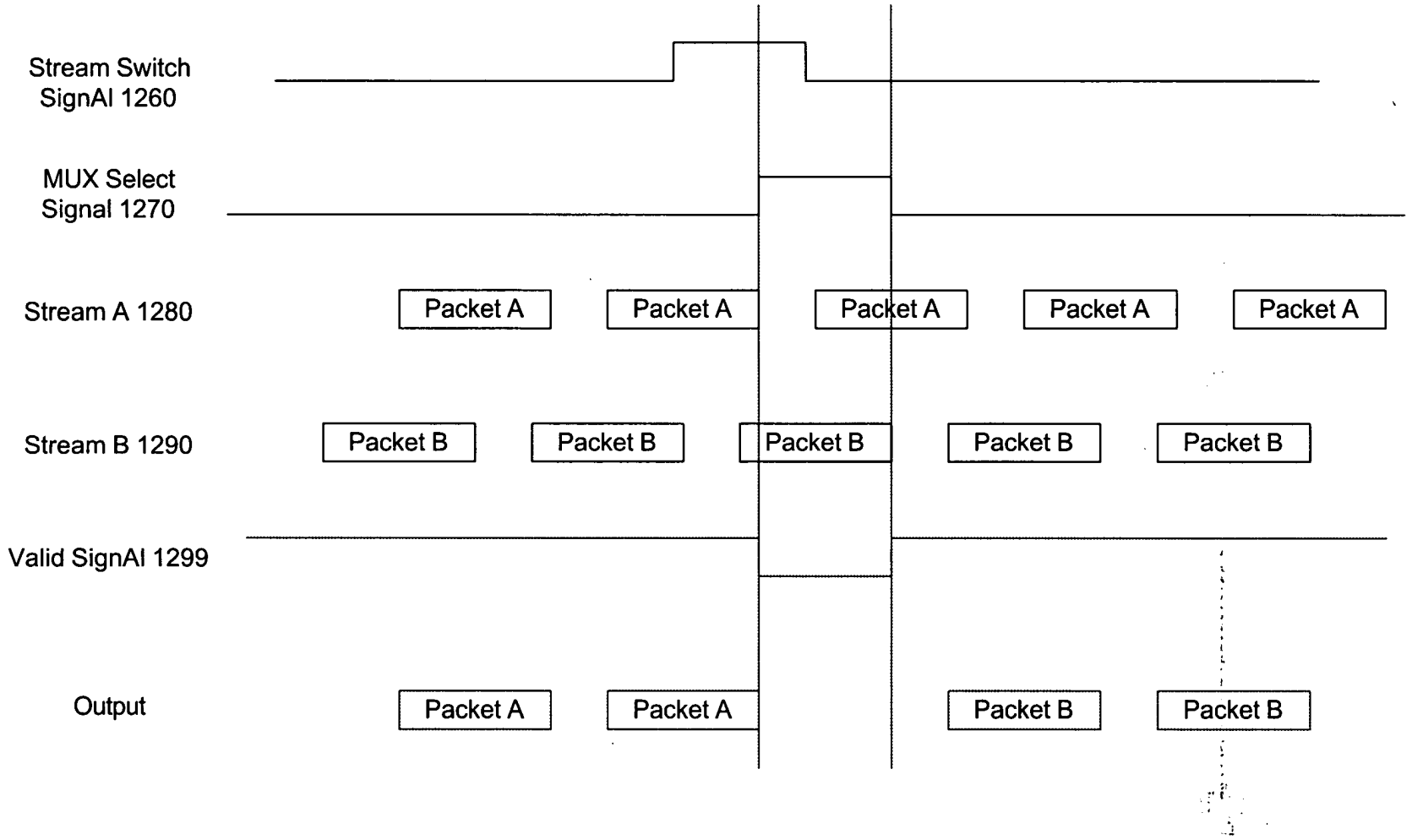

Stream Switch SignAl 1260
MUX Select Signal 1270
Stream A 1280
Packet A
Packet A
Packet A
Packet A
Packet A
Stream B 1290
Packet B
Packet B
Packet B
Packet B
Packet B
Valid SignAl 1299
Output
Packet A
Packet A
Packet B
Packet B

Fig. 12B

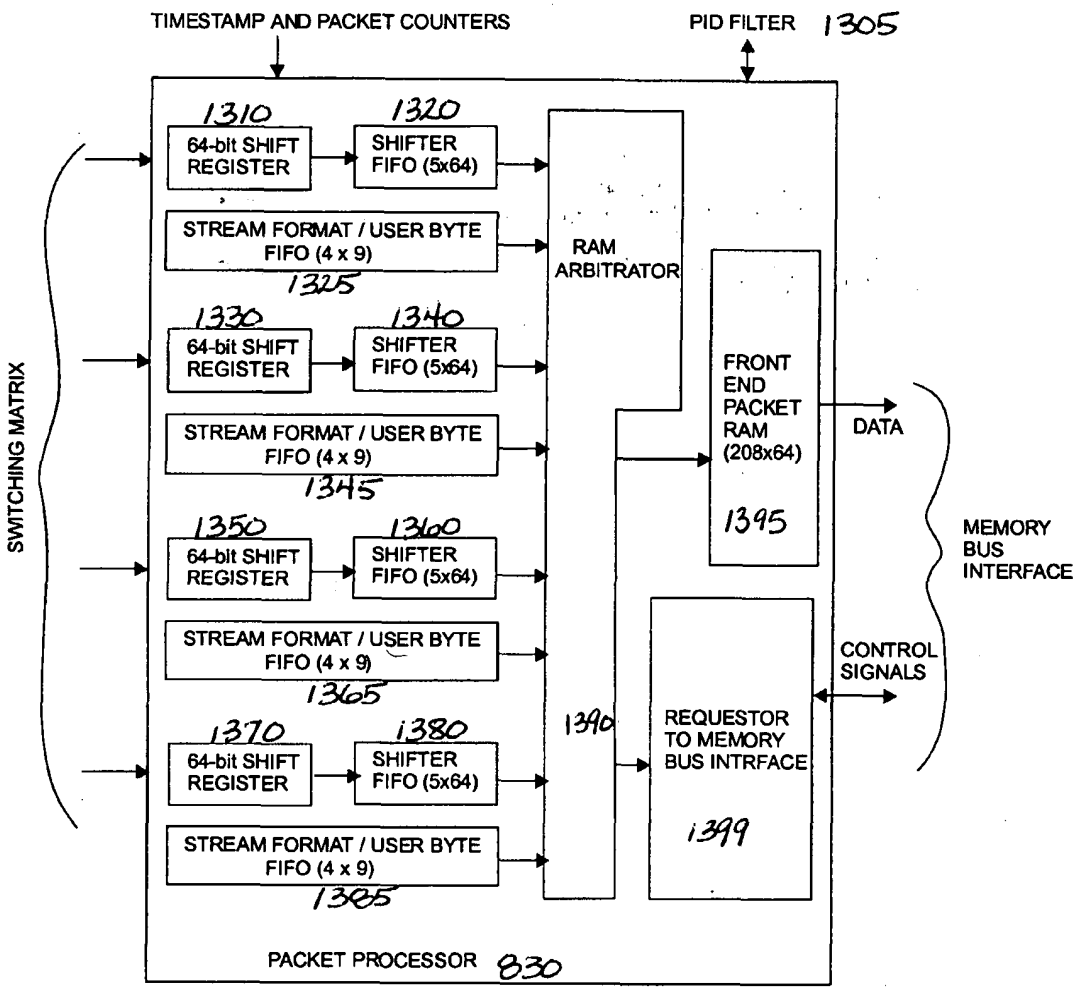

TIMESTAMP AND PACKET COUNTERS
PID FILTER
1305
SWITCHING MATRIX
1310
64-bit SHIFT REGISTER
1320
SHIFTER FIFO (5x64)
STREAM FORMAT / USER BYTE FIFO (4 x 9)
1325
1330
64-bit SHIFT REGISTER
1340
SHIFTER FIFO (5x64)
STREAM FORMAT / USER BYTE FIFO (4 x 9)
1345
1350
64-bit SHIFT REGISTER
1360
SHIFTER FIFO (5x64)
STREAM FORMAT / USER BYTE FIFO (4 x 9)
1365
1370
64-bit SHIFT REGISTER
1380
SHIFTER FIFO (5x64)
STREAM FORMAT / USER BYTE FIFO (4 x 9)
1385
RAM ARBITRATOR
1390
FRONT END PACKET RAM (208x64)
1395
REQUESTOR TO MEMORY BUS INTRFACE
1399
DATA
CONTROL SIGNALS
MEMORY BUS INTERFACE
PACKET PROCESSOR 830

FIGURE 13

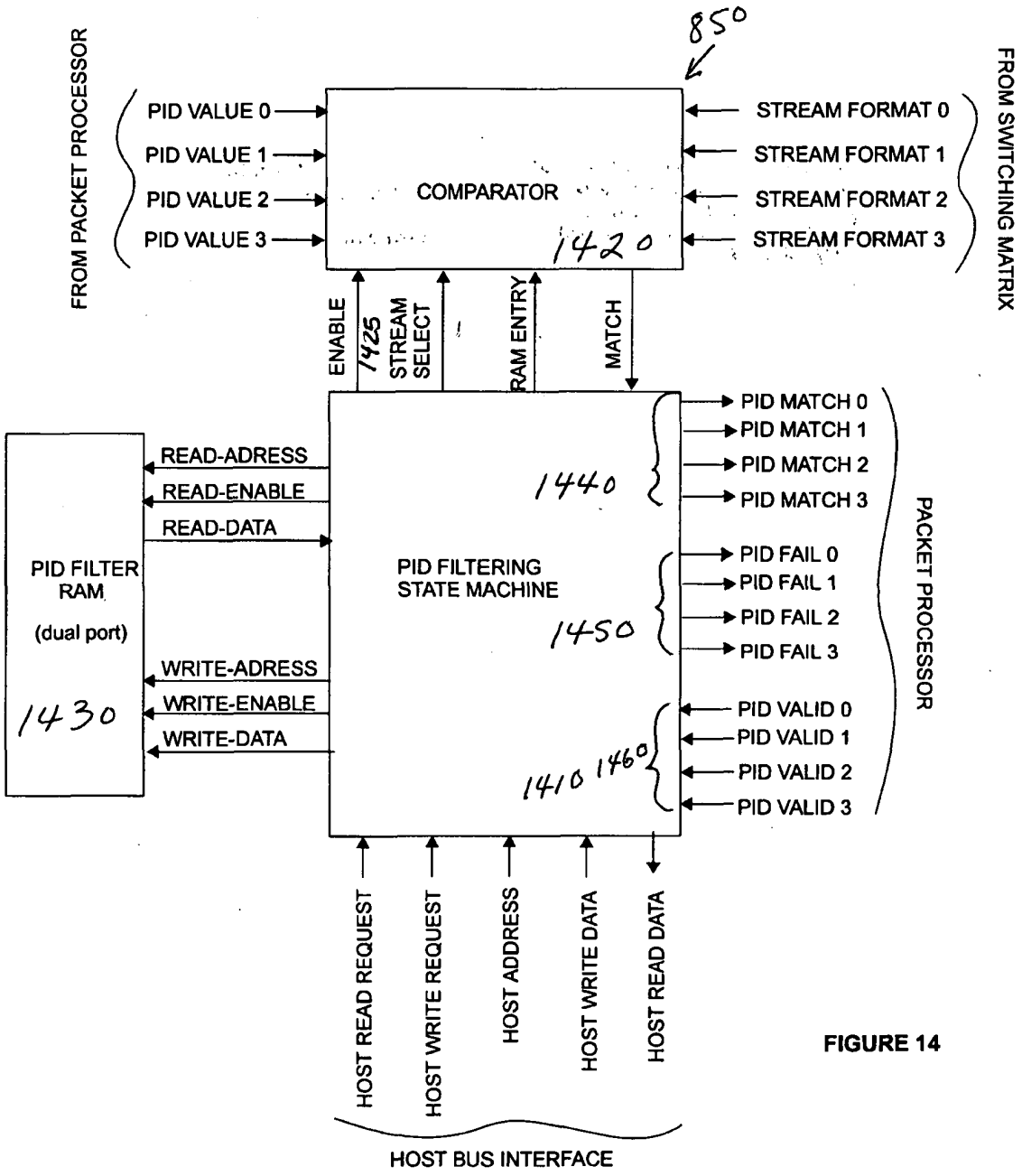

850
FROM PACKET PROCESSOR
PID VALUE 0
PID VALUE 1
PID VALUE 2
PID VALUE 3
COMPARATOR
1420
STREAM FORMAT 0
STREAM FORMAT 1
STREAM FORMAT 2
STREAM FORMAT 3
FROM SWITCHING MATRIX
ENABLE
1425
STREAM SELECT
RAM ENTRY
MATCH
PID FILTER RAM
(dual port)
1430
READ-ADRESS
READ-ENABLE
READ-DATA
WRITE-ADRESS
WRITE-ENABLE
WRITE-DATA
PID FILTERING STATE MACHINE
1440
PID MATCH 0
PID MATCH 1
PID MATCH 2
PID MATCH 3
1450
PID FAIL 0
PID FAIL 1
PID FAIL 2
PID FAIL 3
1410
1460
PID VALID 0
PID VALID 1
PID VALID 2
PID VALID 3
PACKET PROCESSOR
HOST READ REQUEST
HOST WRITE REQUEST
HOST ADDRESS
HOST WRITE DATA
HOST READ DATA
HOST BUS INTERFACE

FIGURE 14

FULL TRANSPORT: PLAYBACK RUNNING AT CONSTANT KNOWN RATE

1510

PARTIAL TRANSPORT: PLAYBACK RUNNING IN TIMESTAMP-PER-PACKET MODE

1520

PARTIAL TRANSPORT: PLAYBACK RUNNING IN TIMESTAMP-PER-CHUNK MODE

1530

■ = CHUNK LEAD PACKET
(typically a PCR Packet)

FIGURE 15

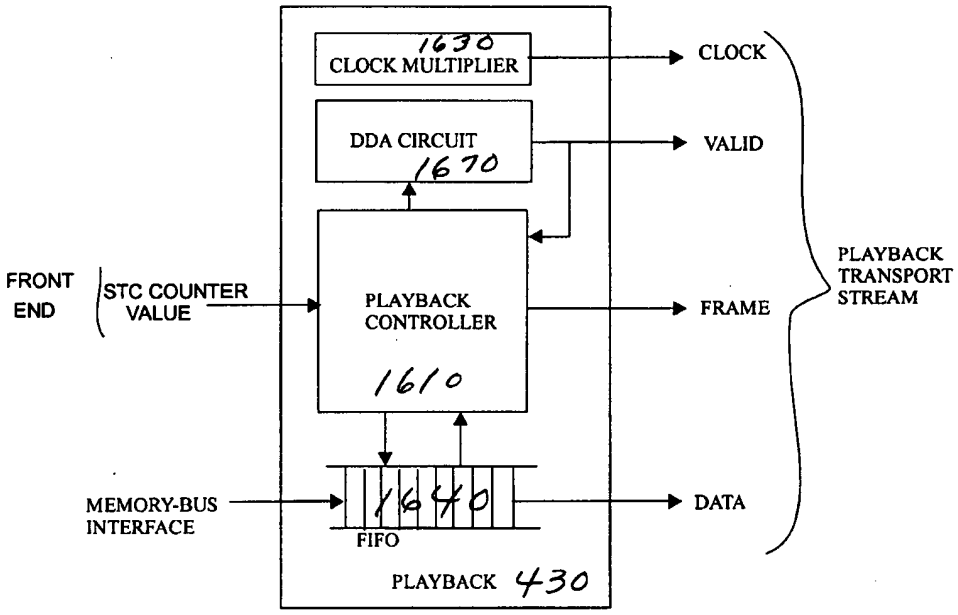


FIGURE 16

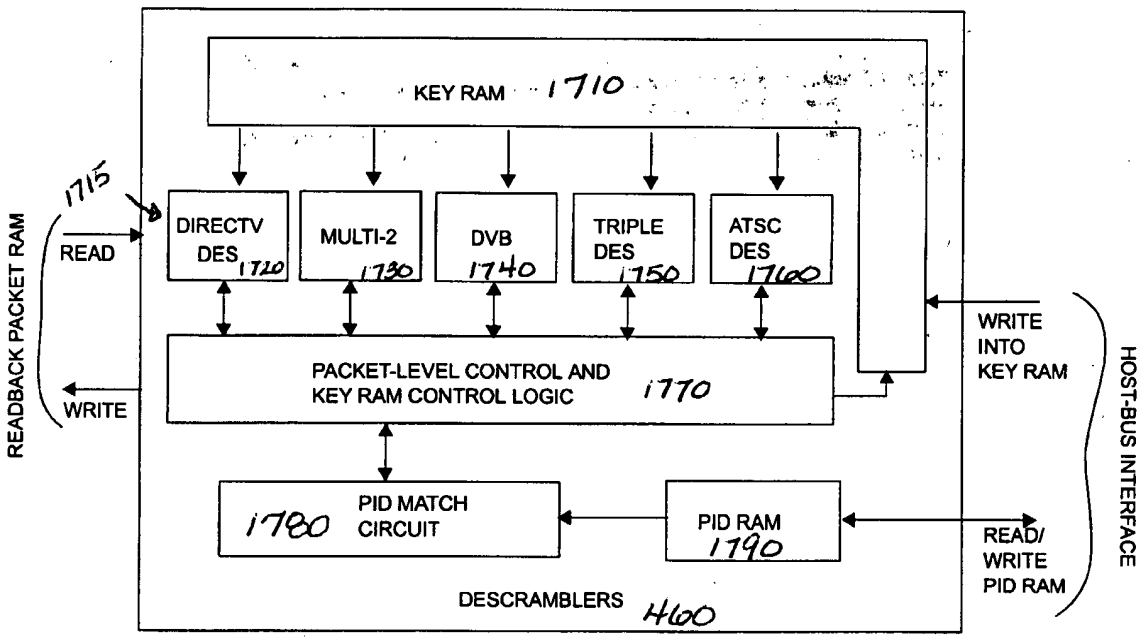

KEY RAM 1710
1715
READ
DIRECTV DES 1720
MULTI-2 1730
DVB 1740
TRIPLE DES 1750
ATSC DES 1760
READBACK PACKET RAM
WRITE
PACKET-LEVEL CONTROL AND KEY RAM CONTROL LOGIC 1770
WRITE INTO KEY RAM
HOST-BUS INTERFACE
1780 PID MATCH CIRCUIT
PID RAM 1790
READ/ WRITE PID RAM
DESCRAMBLERS 460

FIGURE 17

Throughput of the Descrambling Algorithms

Descrambling Algorithm	#cycles per 8 bytes	Thruput 108 MHz (in Mbps)	Thruput 150 MHz (in Mbps)	Thruput 180 MHz (in Mbps)
Multi-2	36	192	267	320
DSS DES-ECB	28	247	343	411
DVB	65	106	148	177
MPEG DES-ECB	28	247	343	411
Triple-DES CBC	72	96	133	160

Number of Streams That Can be Descrambled For Different Broadcasts

Broadcast Type	Algorithm Required	Strm Rate (Mbps)	#Strms Descr 108 MHz	#Strms Descr 150 MHz	#Strms Descr 180 MHz
Europe DVB*	DVB	60			
Terrestrial US	Triple DES	19.4	4.9	6.9	8.2
DirecTV US	DSS DES	38.8	6.4	8.8	8.8
DirecTV Japan**	DVB	40	2.7	3.7	4.4
ARIB BS4 Japan	Multi-2	28.04	6.8	9.5	9.5
ATSC Cable**	Triple DES	38.8			4.1
Echostar US	DVB	24	4.4	6.2	7.4

* 60 Mbps contains close to 10 programs, out of which we would descramble 2 or 3. So the effective rate is more like 20 Mbps.

** Likewise for these cases as well, a stream is packed with numerous programs, and we would descramble only a few.

Number of Streams That Can be Descrambled For Different Broadcasts

Descr	#StdDefnPgms Descr			#HIDefnPgms Descr		
Algorithm	108 MHz	150 MHz	180 MHz	108 MHz	150 MHz	180 MHz
Multi-2	32	44	53	10	14	17
DSS DES	41	57	69	13	18	21
DVB	18	25	30	6	8	9
MPEG DES	41	57	69	13	18	21
Triple-DES	16	22	27	5	7	8

Note: For this table we assume SD-Rate=6Mbps/program
HD-Rate=19.2Mbps/program

FIGURE 18

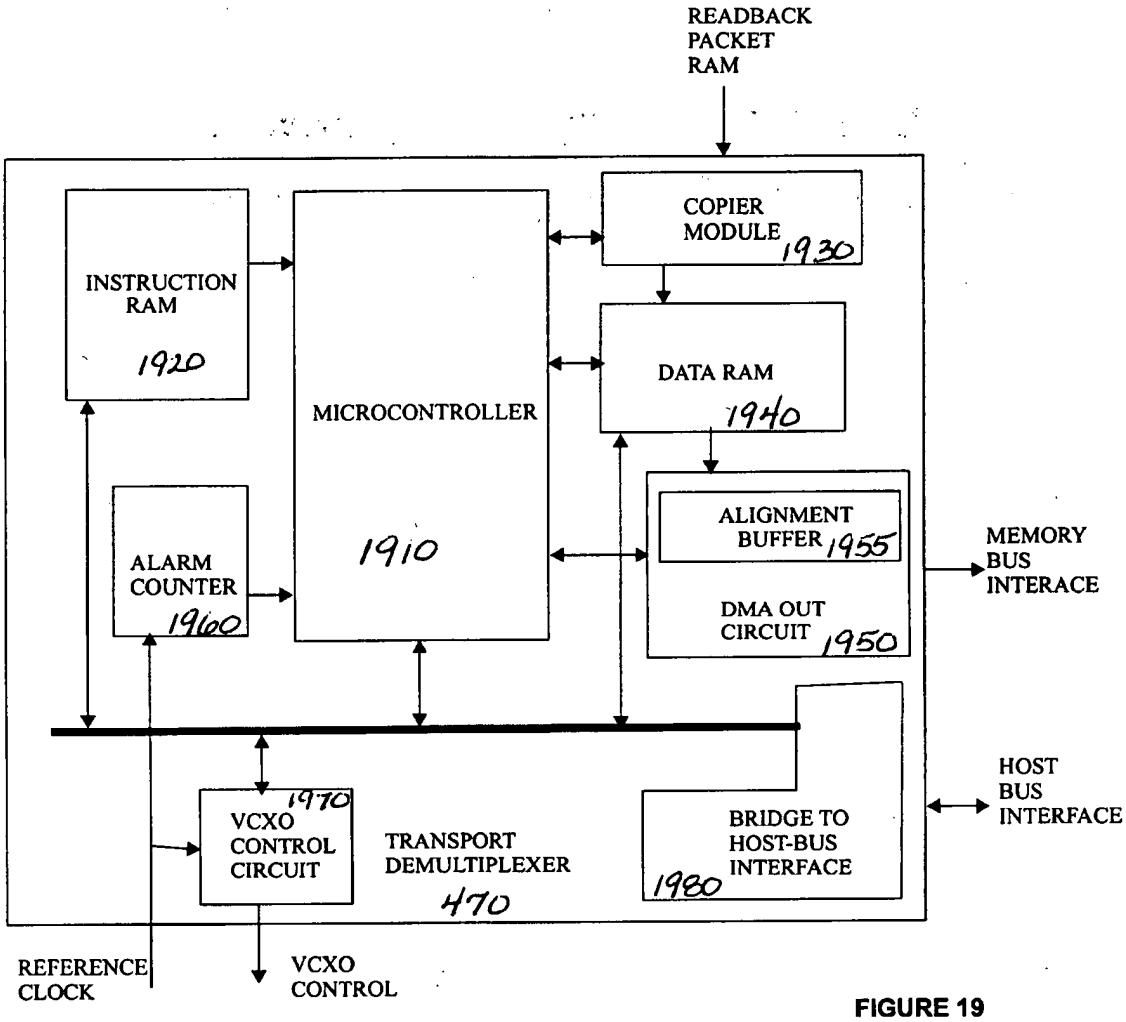
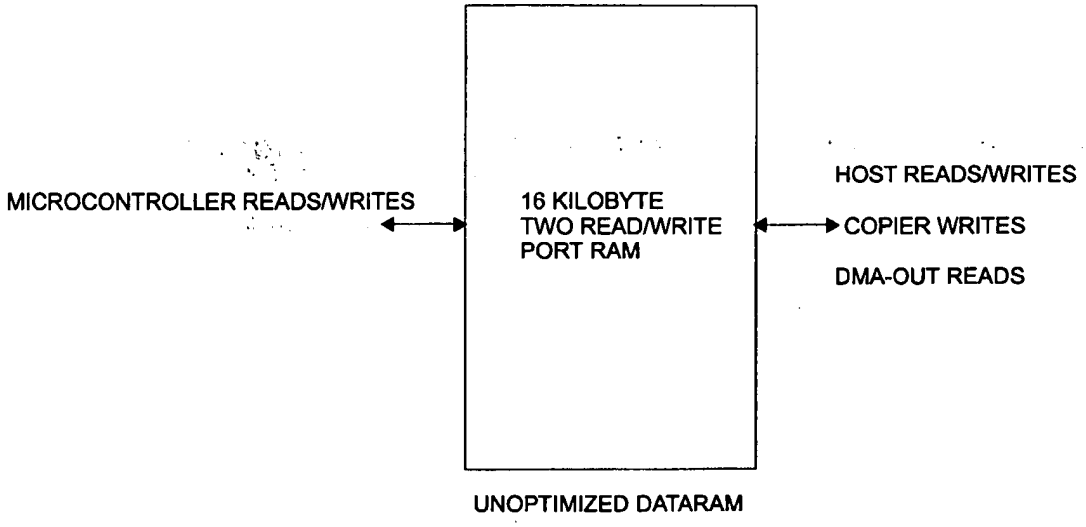

READBACK
PACKET
RAM
INSTRUCTION
RAM
1920
MICROCONTROLLER
1910
COPIER
MODULE
1930
DATA RAM
1940
ALIGNMENT
BUFFER
1955
DMA OUT
CIRCUIT
1950
MEMORY
BUS
INTERACE
ALARM
COUNTER
1960
1970
VCXO
CONTROL
CIRCUIT
TRANSPORT
DEMULTIPLEXER
470
BRIDGE TO
HOST-BUS
INTERFACE
1980
HOST
BUS
INTERFACE
REFERENCE
CLOCK
VCXO
CONTROL

FIGURE 19


MICROCONTROLLER READS/WRITES
16 KILOBYTE
TWO READ/WRITE
PORT RAM
HOST READS/WRITES
COPIER WRITES
DMA-OUT READS
UNOPTIMIZED DATARAM

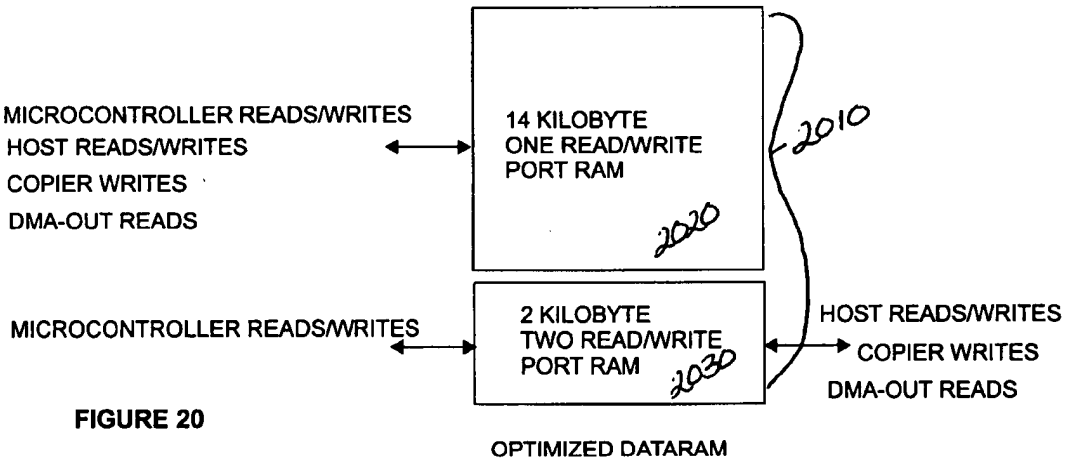

MICROCONTROLLER READS/WRITES
HOST READS/WRITES
COPIER WRITES
DMA-OUT READS
14 KILOBYTE
ONE READ/WRITE
PORT RAM
2020
2010
MICROCONTROLLER READS/WRITES
2 KILOBYTE
TWO READ/WRITE
PORT RAM
2030
HOST READS/WRITES
COPIER WRITES
DMA-OUT READS
OPTIMIZED DATARAM

FIGURE 20